IN THE CLAIMS

Please amend the claims as follows:

1-29. (Canceled)

30. (Currently Amended) A thin-film transistor comprising:

a source region and a drain region which are provided with an interval on an insulating substrate;

a gate insulator layer which is provided over the interval between the source region and the drain region;

a gate electrode which is provided on the gate insulator layer; and

a source electrode and a drain electrode which are provided on the source region and the drain region, respectively, wherein

the gate electrode comprises:

a first ~~metal~~ copper diffusion-preventing layer formed on the gate insulator layer;

a ~~metal~~ copper seed layer formed on the first ~~metal~~ copper diffusion-preventing layer;

a ~~metal~~ copper layer formed on the metal seed layer; and

a second ~~metal~~ copper diffusion-preventing layer covering the exposed surface including the side ~~surface~~ , upper and lower surfaces of the multilayered structure having the ~~metal~~ copper seed layer and the ~~metal~~ copper layer, and wherein

the ~~metal~~ copper seed layer and the ~~metal~~ copper layer are surrounded by the first ~~metal~~ copper diffusion-preventing layer and the second ~~metal~~ copper diffusion-preventing layer, and have a forward tapered cross section.

31. (Previously Presented) The thin-film transistor according to claim 30, wherein the source electrode and the drain electrode comprises:

a third [metal] copper diffusion-preventing layer formed on the source region and the drain region;

a copper wiring layer formed on the third [metal] copper diffusion-preventing layer; and

a fourth [metal] copper diffusion-preventing layer formed to surround the copper wiring layer.

32. (Canceled)

33. (Previously Presented) The thin-film transistor according to claim [[32]] 31, wherein a plurality of the thin-film transistors are arranged to form a matrix, and the thin-film transistors have scanning lines connected to the gate electrodes of the thin-film transistors, and signal lines connected to one of the source electrodes and the drain electrodes of the thin-film transistors, the signal lines being provided such that they are surrounded by the first metal diffusion-preventing layer and the second metal diffusion-preventing layer.

34. (Previously Presented) The thin-film transistor according to claim 30, wherein the insulating substrate is formed of one of glass, a quartz glass, ceramics, and a resin material.

35. (Previously Presented) A thin-film transistor comprising:

a source region and a drain region which are provided with an interval on an insulating substrate:

a gate insulator layer which is provided over the interval between the source region and the drain region;

a gate electrode which is provided on the gate insulator layer; and

a source electrode and a drain electrode which are provided on the source region and the drain region, respectively, wherein

the gate electrode comprises:

a first [metal] copper diffusion-preventing layer formed on the gate insulator layer;

a [metal] copper seed layer formed on the first metal diffusion-preventing layer;

a [metal] copper layer formed on the metal seed layer and having a forward tapered cross section; and

a second [metal] copper diffusion-preventing layer covering the exposed surface including the side [surface], upper and lower surfaces of the multilayered structure having the [metal] copper seed layer, the [metal] copper layer and the first [metal] copper diffusion-preventing layer, and wherein

the [metal] copper seed layer and the [metal] copper layer are surrounded by the first [metal] copper diffusion-preventing layer and the second [metal] copper diffusion-preventing layer.

36. (Previously Presented) The thin-film transistor according to claim 35, wherein the insulating substrate is formed of one of glass, a quartz glass, ceramics, and a resin material.

37. (Currently Amended) A thin-film transistor comprising:

a source region and a drain region which are provided with an interval on an insulating substrate;

a gate insulator layer which is provided over the interval between the source region and the drain region;

a gate electrode which is provided on the gate insulator layer; and

a source electrode and a drain electrode which are provided on the source region and the drain region, respectively, wherein

the gate electrode comprises:

a first ~~metal~~ copper diffusion-preventing layer formed on the gate insulator layer;

a ~~metal~~ copper layer formed on the first ~~metal~~ copper diffusion-preventing layer; and

a second ~~metal~~ copper diffusion-preventing layer covering the exposed surface including the side ~~surface~~ , upper and lower surfaces of the multilayered structure having the ~~metal~~ copper layer and the first ~~metal~~ copper diffusion-preventing layer, and wherein

the ~~metal~~ copper layer is surrounded by the first ~~metal~~ copper diffusion-preventing layer and the second ~~metal~~ copper diffusion-preventing layer, and has a forward tapered cross section.

38. (Previously Presented) The thin-film transistor according to claim 37, wherein the insulating substrate is formed of one of glass, a quartz glass, ceramics, and a resin material.